Claim Amendments

1. (Currently amended) A method for fabricating an extended drain region of a high-voltage transistor comprising:

forming an epitaxial layer on a substrate, the epitaxial layer being of a first conductivity type and having a top surface;

etching the epitaxial layer to form ~~a pair of~~ first and second spaced-apart trenches that define a mesa with first and second sidewall portions;

forming a dielectric layer in each of the trenches, the dielectric layer partially filling each of the trenches and covering the first and second sidewall portions;

filling a remaining portion of the trenches with a conductive material to form first and second field plate members in the first and second trenches, respectively, each of the field plate members being ~~that are~~ insulated from the substrate and the epitaxial layer.

2. (Original) The method of claim 1 further comprising:

forming a source region of the first conductivity type at the top surface of the epitaxial layer, the extended drain region being defined between the source region and the substrate.

3. (Original) The method of claim 2 further comprising:

forming a source electrode connected to the source region and a drain electrode connected to the substrate.

4. (Original) The method of claim 1 wherein the dielectric layer and the field plate members are formed with a reduced spacing between the field plate members

and the epitaxial layer near the top surface of the epitaxial layer as compared to near the substrate.

5. (Original) The method of claim 1 wherein the first conductivity type is n-type.

Claims 6-33 (Previously canceled)

34. (Previously presented) A method for fabricating an extended drain region of a power transistor comprising:

forming an epitaxial layer on a substrate, the epitaxial layer and the substrate being of a first conductivity type;

etching the epitaxial layer to define a mesa having first and second sidewall portions and a top surface;

forming a dielectric material on the first and second sidewall portions;

forming first and second field plate members of a conductive material insulated from the first and second sidewall portions of the mesa, respectively, by the dielectric material.

35. (Previously presented) The method of claim 34 further comprising:

forming a source region of the first conductivity type at the top surface, the extended drain region being defined between the source region and the substrate.

36. (Previously presented) The method of claim 35 further comprising:

forming a source electrode connected to the source region and a drain electrode connected to the substrate.

37. (Previously presented) The method of claim 34 wherein the dielectric material and the field plate members are formed with a reduced spacing between the field plate members and the mesa near the top surface as compared to near the substrate.

38. (Previously presented) The method of claim 34 wherein the first conductivity type is n-type.

39. (Previously presented) The method of claim 34 wherein the mesa is formed with a doping concentration that is lower near the top surface, as compared to near the substrate.

40. (Previously presented) The method of claim 34 wherein the mesa is formed with a linearly graded doping profile.

41. (Previously presented) The method of claim 34 wherein the dielectric material comprises silicon dioxide.

42. (Previously presented) The method of claim 34 wherein the field plate members comprise doped polysilicon.

43. (Previously presented) The method of claim 36 further comprising:

thinning the substrate prior to formation of the drain electrode.

44. (Previously presented) The method of claim 34 wherein the substrate is of the first conductivity type.